A METHOD FOR SUPPORTING IMPROVED BURST TRANSFERS ON A COHERENT BUS

ABSTRACT

In a multiprocessor system, comprising master and slave processors, a cache coherency controller, and address concentration devices; a method for improving coherent data transfers is described. A command transaction is generated, and a subsequent command from an initiator. Tags added to the responses or further request responses, stream on high-speed busses. Snoops and accumulated snoops expand on cacheline requests as each processor separates burst commands into multiple cacheline requests. Address concentrators containing a cacheline queue function, funnel transaction requests to a global serialization device, where a queuing process prioritizes indicia and coordinates the results among the processors. The cache issues a single burst command for each affected line. System coherency, performance, and latency improvements occur. Additional support for burst transfers between coherent processors is provided.